IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applicant	:	Maxim B. Belotserkovsky
Application No.:		10/593,882
Filed	:	September 21, 2006
For	:	METHOD AND APPARATUS FOR USE IN CARRIER RECOVERY IN A COMMUNICATIONS SYSTEM
Examiner	:	Omar J. Ghowrwal
Art Unit	:	2463

APPEAL BRIEF

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May It Please The Honorable Board:

Applicants appeal from the FINAL Office Action dated January 12, 2010, in which claims 1-7 of the above-identified application stand rejected.

Applicant waives an Oral Hearing for this appeal.

Please charge the $540.00 fee for filing this Brief to Deposit Account No. 07-0832.

Please charge any additional fee or credit overpayment to the above-indicated Deposit Account.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest of Application No. 10/593,882 is:

Thomson Licensing
1, rue Jeanne d'Arc
92443 Issy-les-Moulineaux Cedex
France

II. RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

III. STATUS OF THE CLAIMS

Claims 1-7 are pending in this application.

Claims 1-7 have been rejected.

The rejection of claims 1-7 are appealed.

IV. STATUS OF AMENDMENTS

In response to the FINAL Office Action dated January 12, 2010, Applicant's representative filed a Notice of Appeal on July 6, 2010 along with a three month extension of time.

This appeal is directed to the claims as they stood at the time of the FINAL Office Action dated January 12, 2010 and which are shown in the Claims Appendix of this Brief.

V. SUMMARY OF CLAIMED SUBJECT MATTER

There are two independent claims pending in this application: claims 1 and 5.

As noted in the background of Applicant's specification, a carrier recovery loop, or carrier tracking loop, is a typical component of a communications system. The carrier recovery loop is a form of phase locked loop (PLL). When the carrier frequency offset, i.e., the frequency difference between the carrier of the received signal and the recovered carrier, is outside the "lock range" of the loop, the so-called "pull-in" process occurs, in which, under proper operating conditions, the loop operates to reduce the carrier frequency offset until the carrier frequency offset falls inside the lock range of the loop and phase lock follows. (Applicant's specification, p. 1, lns. 6-7, 11-15.)

Unfortunately, there will be instances when the "pull-in" process will result in the loop either drifting without any predictable pattern or stabilizing at a false value (a "false-lock" condition). In this regard, an application of Applicant's inventive concept is directed toward detecting a "false lock" condition. (Applicant's specification, p. 8, lns. 28-31.)

In particular, Applicant's independent claim 1 is directed to a method for processing a received signal with a phase-locked loop (PLL) (e.g., CTL 320 of FIG. 5, FIG. 6); generating a carrier frequency offset estimate as a function of a phase error signal of the PLL (steps 555, 560 and 565 of FIG. 8); and detecting a false lock condition as a function of comparing the carrier frequency offset estimate to a closed loop value of the PLL (steps 550, 570 and 575 of FIG. 8). (Applicant's specification, p. 6, lns. 26-27; p. 8, ln. 33 to p. 9, ln. 12.)

Applicant's remaining independent claim 5 is an apparatus claim directed to a carrier tracking loop (CTL) for processing a received signal (e.g., CTL 320 of FIG. 5, FIG. 6); and a processor for estimating a carrier frequency offset as a function of a phase error signal of the CTL (e.g., processor 350 of FIG. 5; steps 555, 560 and 565 of FIG. 8); wherein the processor detects a false lock condition as a function of comparing the estimate of the carrier frequency offset to a closed loop value of the CTL (steps 550, 570 and 575 of FIG. 8). (Applicant's specification, p. 6, lns. 26-27; p. 8, ln. 33 to p. 9, ln. 12.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There are three grounds of rejection to be reviewed on Appeal.

(1) Whether claims 1, 4 and 5 are unpatentable under 35 U.S.C. §103(a) over U.S. Publication No. 2002/0067778 published June 6, 2002 to Ahn (*Ahn*) in view of U.S. Patent No. 5,490,176 issued February 6, 1996 to Peltier (*Peltier*).

(2) Whether claims 2, 3 and 6 are unpatentable under 35 U.S.C. §103(a) over *Ahn* in view of *Peltier* and further in view of "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to Matzner et al. (*Matzner*).

(3) Whether claim 7 is unpatentable under 35 U.S.C. §103(a) over *Ahn* in view of *Peltier* and further in view of U.S. Publication No. 2002/0122511 published September 5, 2002 to Kwentus et al.

VII. ARGUMENT

Rejection of claims 1, 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over U.S. Publication No. 2002/0067778 published June 6, 2002 to Ahn (*Ahn*) in view of U.S. Patent No. 5,490,176 issued February 6, 1996 to Peltier (*Peltier*).

CLAIMS 1, 4 and 5

Independent claims 1 and 5 are patentable over U.S. Publication No. 2002/0067778 published June 6, 2002 to Ahn (*Ahn*) in view of U.S. Patent No. 5,490,176 issued February 6, 1996 to *Peltier* (*Peltier*).

Applicant's dependent claim 4 stands or falls with respective independent claim 1.

INDEPENDENT CLAIMS 1 and 5 ARE PATENTABLE

The combination of *Ahn* and *Peltier* does not yield Applicant's claimed invention for any one of a number of reasons.

At the outset, the Examiner states that *Ahn* describes comparing the frequency offset to a closed loop value of the PLL or CTL as required by Applicant's independent claims 1 and 5 with reference to element 104-3 of FIG. 5, of *Ahn*. Respectfully, the Examiner is wrong. At the outset, this portion of Applicant's claims 1 and 5 require "comparing". However, mere reference to FIG. 13 of *Ahn*, which illustrates element 104-3, and which is shown below

FIG. 13

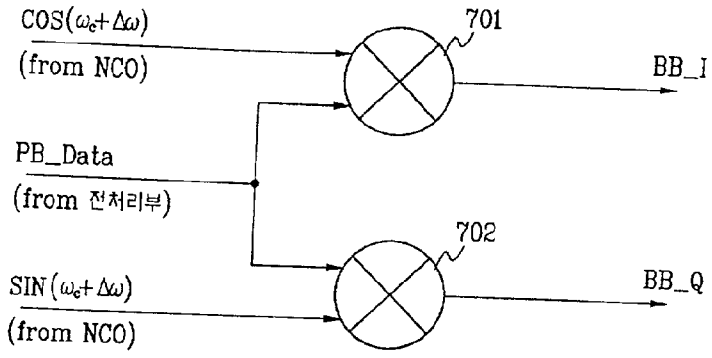

FIG. 13 of *Ahn*

clearly shows there is no comparator – only multipliers 701 and 702. Thus, it is not possible for element 104-3 of *Ahn* to compare anything – let alone Applicant's claimed requirement of comparing the frequency offset to a closed loop value of the PLL or CTL. In view of this, the combination of *Ahn* and *Peltier* does not yield Applicant's claimed invention.

Further, the Examiner's response that the multiplier in *Ahn* performs a comparison is simply wrong for a number of reasons. In particular, the Examiner states that:

> it is known that in order to perform a multiplication, the two terms involved must be compared to one another in or to produce a resulting product. In this case the terms are compared pertaining to the mathematical operations used in multiplication, i.e., a digit of the first term is compared to another digit of the second term during the multiplication operation (a*b = "c", where "c" depends upon the comparison of "a' and "b" in term of multiplication rules).
>
> Final Office Action, p. 2, emphasis added.

First, the word "comparing" in plain English means to examine two or more objects in order to note similarities and differences. Indeed, Applicant's independent claims require "comparing" two items – the carrier frequency offset estimate and a closed loop value of the PLL. In contrast, multiplication does not perform a comparison – especially the multipliers described, and shown in, *Ahn*. The multipliers in *Ahn* simply multiply two inputs together to provide an output. Nowhere does *Ahn* describe, or show, that the inputs are compared to note similarities and differences during the multiplication process. The multipliers described, and shown, in *Ahn*, do not care what the similarities and differences are between the inputs – since the inputs are simply multiplied together as clearly shown in FIG. 13 of *Ahn*.

Second, the Examiner's characterization that "a digit of the first term is compared to another digit of the second term during the multiplication operation" is simply wrong. In multiplication, Applicant asserts that the correct statement is that a digit of the first term is SCALED to another digit of the second term during the multiplication operation. There is no comparison.

Third, for the Examiner to take the position that multiplication involves a comparison not only goes beyond the plain language meaning of comparing but also inappropriately redefines the meaning of multiplication without any support – other than the Examiner's statement "it is known". Absent providing prior art that shows that in

order to perform a multiplication as shown in FIG. 13, of *Ahn*, you must "compare" the numbers against each other – this argument must fail.

Fourth, one skilled in the art is not going to look at the multipliers 701 and 702 shown in FIG. 13, of *Ahn*, and see a comparator. Applicant submits that one skilled in the art would only see multipliers in FIG. 13, of *Ahn*.

Finally, the Examiner refers to "the mathematical operations used in multiplication" – what are the mathematical operations? Applicant respectfully submits there is only one mathematical operation – namely multiplication. There is no comparison.

In view of the above, Applicant maintains that FIG. 13, of *Ahn*, does not describe or suggest, comparing the frequency offset to a closed loop value of the PLL or CTL as required by Applicant's independent claims 1 and 5. As such, just on this fact alone, the combination of *Ahn* and *Peltier* does not yield Applicant's claimed invention.

However, *Peltier* also has deficiencies. In particular, the Examiner states that *Peltier* describes that a

> false lock is detected when the phase offset changes sign (abstract, col. 5, lines 10-30, claim 1), i.e. an offset signal is compared to a previous offset value.
>
> Office Action, 8/11/09, p. 4; emphasis added.

Respectfully, the Examiner is mischaracterizing *Peltier*. This portion of *Peltier* describes the operation of the circuits shown in FIGs. 2 and 3, of *Peltier*. In particular, *Peltier* describes generating two clock signals and comparing the **phase offset** between these two clock signals. (*Peltier*, FIGs. 5a and 5b, col. 2, lns. 34-35; claim 1.) Thus, there is no offset signal nor a previous offset value described in *Peltier* as asserted by the Examiner – just comparing the **phase offset** BETWEEN two clock signals. This, in fact, is clearly shown in FIG. 3, of *Peltier*, shown below (the same analysis applies to FIG. 2, of *Peltier*):

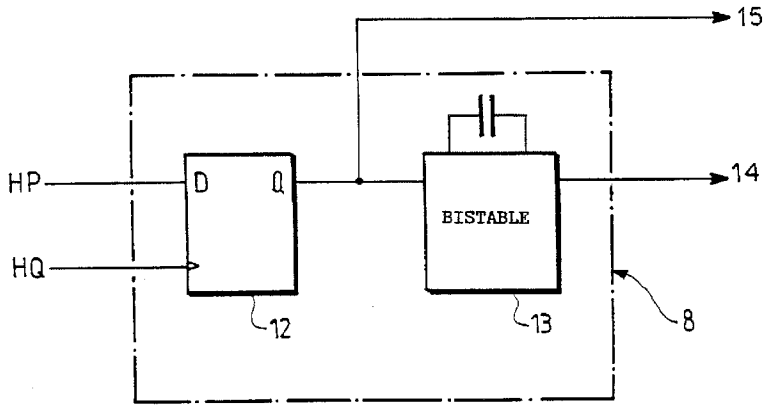

FIG. 3

FIG. 3 of *Peltier*

In FIG. 3, of *Peltier*, it should be noted that element 12 is simply a D-Flip Flop. (*Peltier*, col. 4, ln. 53.) As such, the signal "HQ" (on the clock input of element 12) simply clocks in the value of signal "HP" (on the D input of element 12) to the Q output of element 12. Both signal "HQ" and signal "HP" are separate clock signals. (*Peltier*, col. 4, lns. 22-24.) Since "HQ" and "HP" are digital signals, the D-Flip Flop merely latches in the corresponding value of the "HP" clock signal when the "HQ" clock signal goes "high". (*Peltier*, col. 4, ln. 61, to col. 5, ln. 30.) Thus, the "HQ" clock signal simply samples the "HP" clock signal. Further, since "HQ" and "HP" are separate clock signals – neither one is a carrier frequency offset estimate or a closed loop value of a PLL or CTL as required by Applicant's independent claims 1 and 5. In fact, the Q output of the D-Flip Flop shown in FIG. 3, of *Peltier*, only indicates the phase difference between the "HQ" and "HP" signals – there is no carrier **frequency** offset estimate. (*Peltier*, col. 4, lns. 61-63; col. 5, lns. 10-13.) As such, *Peltier* has nothing to do with Applicant's claimed invention where a false lock is detected by comparing a carrier frequency offset estimate to a closed loop value of a phase-locked loop as required by Applicant's independent claims 1 and 5. In view of this, the combination of *Ahn* and *Peltier* again does not yield Applicant's claimed invention.

As a result of all the above, Applicant's independent claims 1 and 5 are patentable over the *Ahn* in view of *Peltier*. Thus, Applicant's dependent claim 4 is also in condition for allowance.

Rejection of Dependent Claims 2, 3 and 6 under 35 U.S.C. §103(a) as being unpatentable over *Ahn* in view of *Peltier* and further in view of "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to Matzner et al.

DEPENDENT CLAIMS 2, 3 and 6

If the rejection of independent claims 1 and 5 fall, then respective dependent claims 2, 3 and 6 are patentable. As such, the rejections of dependent claims 2, 3 and 6 stand or fall with their respective independent claims.

Rejection of Dependent Claim 7 under 35 U.S.C. §103(a) as being unpatentable over *Ahn* in view of *Peltier* and further in view of U.S. Publication No. 2002/0122511 published September 5, 2002 to Kwentus et al.

DEPENDENT CLAIM 7

If the rejection of independent claim 5 falls, then respective dependent claim 7 is patentable. As such, the rejection of dependent claim 7 stands or falls with independent claim 5.

VIII. CONCLUSION

For the above reasons, Applicant submits that claims 1-7 are patentable. It is therefore respectfully requested that:

- the rejection of claims 1, 4 and 5 under 35 U.S.C. § 103(a);
- the rejection of dependent claims 2, 3 and 6 under 35 U.S.C. § 103(a); and
- the rejection of dependent claim 7 under 35 U.S.C. § 103(a);

all be reversed.

Respectfully submitted,

Maxim B. Belotserkovsky

By /Joseph J. Opalach/

Joseph J. Opalach
Registration No.: 36,229
(609) 734-6839

Patent Operations
Thomson Licensing LLC.
P.O. Box 5312
Princeton, New Jersey 08543-5312

September 1, 2010

IX. CLAIMS APPENDIX

1. (Previously presented) A method for use in a receiver, the method comprising:

using the receiver to perform the steps of

processing a received signal with a phase-locked loop (PLL);

generating a carrier frequency offset estimate as a function of a phase error signal of the PLL; and

detecting a false lock condition as a function of comparing the carrier frequency offset estimate to a closed loop value of the PLL.

2. (Original) The method of claim 1, wherein the processing step includes the step of setting the PLL in an open loop mode of operation.

3. (Original) The method of claim 1, wherein the generating step includes the steps of:

determining a rollover count value for the phase error signal;

determining a symbol count value of the received signal; and

generating the carrier frequency offset estimate from the determined rollover count value and determined symbol count value.

4. (Original) The method of claim 1, further comprising the step of updating the PLL with the carrier frequency offset estimate.

5. (Original) A receiver comprising:

a carrier tracking loop (CTL) for processing a received signal; and

a processor for estimating a carrier frequency offset as a function of a phase error signal of the CTL;

wherein the processor detects a false lock condition as a function of comparing the estimate of the carrier frequency offset to a closed loop value of the CTL.

6. (Original) The receiver of claim 5, wherein the CTL includes a rollover counter and a symbol counter accessible by the processor for use in estimating the carrier frequency offset.

7. (Previously presented) The receiver of claim 5, wherein the receiver is a set-top box.

8. (Canceled).

X. EVIDENCE APPENDIX (**NONE**)

None.

XI. RELATED PROCEEDINGS APPENDIX (**NONE**)

None.